We claim:

1. A semiconductor structure, comprising:

a polycrystalline layer; and

a rough layer formed from an undoped silicon, the rough layer being formed on the polycrystalline layer and including protrusions extending from a surface of the layer.

2. The semiconductor structure of claim 1, wherein the protrusions include hemispherical protrusions.

3. The semiconductor structure of claim 1, wherein the polycrystalline layer comprises a conductive polycrystalline material.

4. The semiconductor structure of claim 1, wherein the polycrystalline layer comprises a conductive alloy that becomes polycrystalline at a temperature greater than about 500 degrees Celsius.

5. The semiconductor structure of claim 1, wherein the polycrystalline layer comprises a bottom electrode of a capacitor and wherein the protrusions of the rough layer increase the surface area of the bottom electrode so as to increase the capacitance of the capacitor.

6. A capacitor, comprising:

a top electrode;

a dielectric coupled to the top electrode; and

a bottom electrode coupled to the dielectric, wherein the bottom electrode includes a rough layer and an electrode layer, wherein the rough layer includes hemispherical protrusions formed from undoped silicon, and wherein the electrode layer is formed from a polycrystalline material.

7. The capacitor of claim 6, wherein the electrode layer of the bottom electrode forms an outer surface of the capacitor, and wherein the rough layer forms an inner surface of the capacitor.

8. The capacitor of claim 6, wherein the bottom electrode comprises an outer surface, an embedded layer, and an inner surface to define a container structure, wherein the rough layer defines the inner surface and the outer surface, and wherein the relatively smooth surface defines the embedded layer.

9. The capacitor of claim 6, wherein the undoped silicon includes undoped amorphous silicon.

10. The capacitor of claim 6, wherein the electrode layer is a polycrystalline alloy selected from a combination of silicon and germanium.

11. A semiconductor structure, comprising:

a first capacitor having a bottom electrode having an outer surface and an inner surface, wherein the outer surface of the bottom electrode of the first capacitor is smooth, and wherein the inner surface of the bottom electrode of the first capacitor is rough from a number of hemispherical protrusions; and

a second capacitor having a bottom electrode having an outer surface and an inner surface, wherein the outer surface of the bottom electrode of the second capacitor is smooth and is near the outer surface of the bottom electrode of the first capacitor such that the first and the second capacitor exists in close proximity without shorting, and wherein the inner surface of the bottom electrode of the second capacitor is rough from a number of hemispherical protrusions.

12. The semiconductor structure of claim 11, wherein a portion of the outer surface of the bottom electrode of the first capacitor is housed in a nonconductive material so as

to expose the rest of the outer surface of the bottom electrode of the first capacitor, and wherein a portion of the outer surface of the bottom electrode of the second capacitor is housed in the nonconductive material so as to expose the rest of the outer surface of the bottom electrode of the second capacitor.

13. The semiconductor structure of claim 11, wherein the outer surfaces of the bottom electrodes of the first and second capacitors are composed of a material selected from undoped silicon.

14. The semiconductor structure of claim 11, wherein the inner surfaces of the bottom electrodes of the first and second capacitors are composed of a material selected from polycrystalline silicon-germanium.

15. The semiconductor structure of claim 11, wherein the first capacitor includes a first dielectric layer that overlies the bottom electrode of the first capacitor and a first top electrode that overlies the first dielectric layer, and wherein the second capacitor includes a second dielectric layer that overlies the bottom electrode of the second capacitor and a second top electrode that overlies the second dielectric layer.

16. A method for making a semiconductor structure, comprising:

forming a polycrystalline layer ; and

forming hemispherical protrusions in an undoped silicon layer that overlies the polycrystalline layer.

17. The method of claim 16, wherein forming a polycrystalline layer includes forming a silicon-germanium alloy.

18. The method of claim 16, wherein forming hemispherical protrusions includes depositing the undoped silicon layer by using low-pressure chemical vapor deposition of

silane gas at a temperature less than about 550 degrees Celsius and greater than about 450 degrees Celsius.

19. The method of claim 18, wherein forming hemispherical protrusions includes forming atomic seeds from which hemispherical protrusions are grown by chemical vapor deposition of silane gas at a temperature less than about 600 degrees Celsius and greater than about 550 degrees Celsius.

20. The method of claim 19, wherein forming hemispherical protrusions includes annealing so as to grow the atomic seeds to form hemispherical protrusions.

21. A method for making a semiconductor structure, comprising:

forming a silicon-germanium alloy layer;

forming an undoped silicon layer that overlies the silicon-germanium alloy layer;

seeding the undoped silicon layer to cluster atoms and thereby form nuclei on a surface of the undoped silicon layer; and

annealing the semiconductor structure to grow the nuclei into hemispherical protrusions.

22. The method of claim 21, wherein forming a silicon-germanium alloy layer includes flowing silane gas, phosphate gas, and germanium source gas at a temperature greater than about 500 degrees Celsius.

23. The method of claim 21, wherein forming an undoped silicon layer includes flowing silane gas at a temperature greater than about 300 degrees Celsius and less than about 550 degrees Celsius.

24. The method of claim 21, wherein seeding includes flowing silane gas at a temperature greater than about 550 degrees Celsius and less than about 600 degrees Celsius,

wherein a flow rate of silane gas includes greater than about 10 standard cubic centimeters per minute and less than about 30 standard cubic centimeters per minute.

25. The method of claim 21, wherein annealing includes annealing at a temperature greater than about 550 degrees Celsius and less than about 600 degrees Celsius.

26. The method of claim 21, further comprising planarizing the semiconductor structure using a chemical mechanical planarization technique.

27. The method of claim 26, further comprising etching using an etch back technique to remove a portion of borophosphorus silicate glass that surrounds the container.

28. A method for making a semiconductor structure, comprising:

forming a container in a layer of borophosphorus silicate glass (BPSG);

forming a silicon-germanium alloy layer on a surface of the container and on a surface of the BPSG layer;

forming an undoped silicon layer that overlies the silicon-germanium alloy layer;

removing the portions of the silicon-germanium alloy and undoped silicon layer that are lying on a surface of the BPSG layer;

removing a portion of the BPSG to expose an outer surface of the silicon-germanium alloy layer; and

forming hemispherical protrusions on a surface of the undoped silicone layer.

29. The method of claim 28, wherein removing the portions of the silicon-germanium alloy and undoped silicon layer includes chemical-mechanical planarizing.

30. The method of claim 29, wherein forming hemispherical protrusions includes annealing the semiconductor structure to grow the nuclei into hemispherical protrusions.

31. The method of claim 30, wherein annealing includes annealing at a temperature greater than about 600 degrees Celsius and less than about 650 degrees Celsius for about 5 minutes.

32. The method of claim 31, wherein seeding includes flowing silane gas at a rate of about 15 standard cubic centimeters per minute.

33. A method for making a semiconductor structure, comprising:

forming a container in a layer of borophosphorus silicate glass (BPSG);

forming a silicon-germanium alloy layer on a surface of the container, the silicon-germanium alloy having an outer surface abutting the BPSG layer and having an inner surface;

removing portions of the silicon-germanium alloy overlying a surface of the BPSG layer;

removing portions of the BPSG layer to expose at least a portion of the outer surface of the silicon-germanium layer;

depositing an undoped silicon layer over the inner surface and exposed outer surface of the silicon-germanium alloy layer; and

converting the undoped silicon layer into hemispherical protrusions.

34. The method of claim 33, wherein converting includes seeding the undoped silicon layer to cluster atoms to form nuclei.

35. The method of claim 34, wherein converting includes annealing the semiconductor structure to grow the nuclei into hemispherical protrusions.

36. The method of claim 34, further comprising depositing a dielectric layer over the hemispherical protrusions, and wherein the dielectric layer conforms to the hemispherical protrusions.

37. The method of claim 36, further comprising depositing a conductive layer over the dielectric layer, and wherein the silicon-germanium alloy, the dielectric layer and the conductive layer define a capacitor structure.

38. A semiconductor structure, comprising:

a first layer formed from an undoped substance and including first and second surfaces, the first surface including a plurality of surface protrusions that increase a surface area of the first layer; and

a second layer formed abutting the second surface of the first layer and including a plurality of atoms, the atoms in the second layer being sufficiently bound in the second layer to substantially remain in the second layer during formation of the first layer.

39. The semiconductor structure of claim 38, wherein the first layer comprises an undoped silicon layer.

40. The semiconductor structure of claim 38 wherein the undoped silicon layer comprises an undoped amorphous silicon layer.

41. The semiconductor structure of claim 38 wherein the second layer comprises a polycrystalline layer.

42. A capacitor, comprising:

a first electrode layer having first and second surfaces formed from undoped silicon;

first and second rough layers formed on the first and second surfaces of the first electrode layer, respectively, each of the first and second rough layers including a plurality of surface protrusions that increase a corresponding surface area of the layer;

a dielectric layer formed on the first and second HSG layers; and

a second electrode layer formed on the dielectric layer.

43. The capacitor of claim 42, wherein the first electrode layer comprises a polycrystalline layer.

44. The capacitor of claim 42, wherein the first and second rough layers comprise first and second HSG layers, respectively.

45. The capacitor of claim 42, wherein the first rough layer is formed over substantially the entire first surface of the first electrode layer and wherein the second rough layer comprises a segment formed on a first portion of the second surface of the first electrode layer and another segment formed on a second portion of the second surface of the first electrode layer.

46. The capacitor of claim 43, wherein the first electrode layer comprises a U-shaped structure and the first surface corresponds to an inner surface and the second surface corresponds to an outer surface.

47. A capacitor, comprising:

a first electrode layer having first and second surfaces formed from undoped silicon;

a rough layer formed on the first surface of the first electrode layer, the rough layer including a plurality of surface protrusions that increase a corresponding surface area of the layer;

a dielectric layer formed on the rough layer and on the second surface of the first electrode layer; and

a second electrode layer formed on the dielectric layer.

48. The capacitor of claim 47, wherein the first electrode layer comprises a polycrystalline layer.

49. The capacitor of claim 47, wherein the first and second rough layers comprise first and second HSG layers, respectively.

50. The capacitor of claim 47, wherein the dielectric layer comprises a first segment formed on a first portion of the second surface of the first electrode layer and a second segment formed on a second portion of the second surface of the first electrode layer.

51. The capacitor of claim 47, wherein the first electrode layer comprises a U-shaped structure and the first surface corresponds to an inner surface and the second surface corresponds to an outer surface.